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(71) Applicant(s)
NEC Technologies (UK) Ltd
(Incorporated in the United Kingdom)
Level 3, The Imperium, Imperial Way, READING,
Berks, RG2 0TD, United Kingdom

(72) Inventor(s)
David Cooper

(74) Agent and/or Address for Service
NEC Technologies (UK) Ltd
Level 3, The Imperium, Imperial Way, READING,
Berks, RG2 0TD, United Kingdom

(54) Abstract Title
High resolution clock reconstruction for use in a mobile telecommunication device

(57) A mobile telecommunication device such as a mobile phone includes a high frequency, high accuracy clock oscillator 20 and a high resolution counter 22 for counting pulses from the main oscillator for controlling the timing of communication operations. A continuously running secondary low frequency clock oscillator 25 is provided for timing sleep intervals when the main oscillator is switched off for power saving purposes. Counters 27, 28 are provided for cyclically switching the main oscillator on and off periodically for time intervals determined by the secondary clock. Means 23, 24 is provided for loading the high resolution counter with a restart value at the commencement of the on phase of each cycle, the restart value being determined in accordance with the restart value in the previous cycle and the total time elapsed since the previous start.

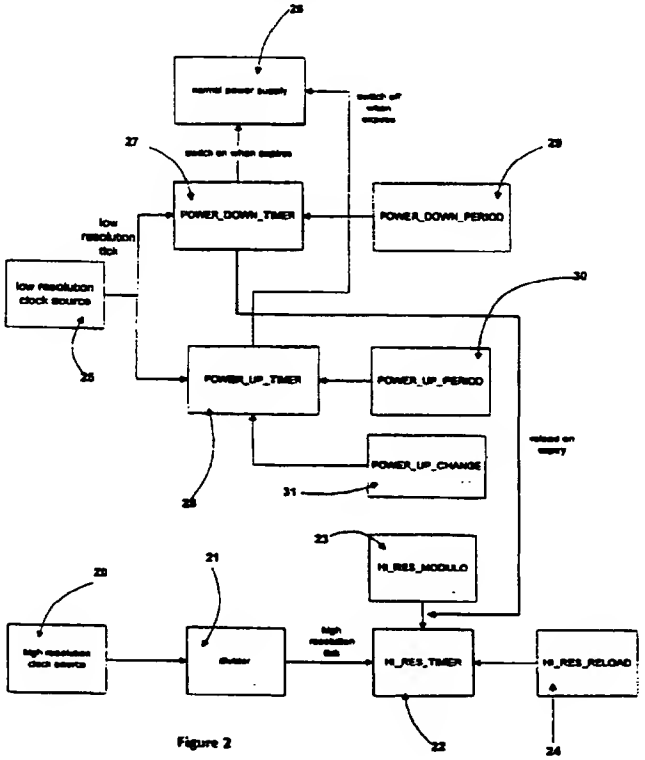

Figure 2

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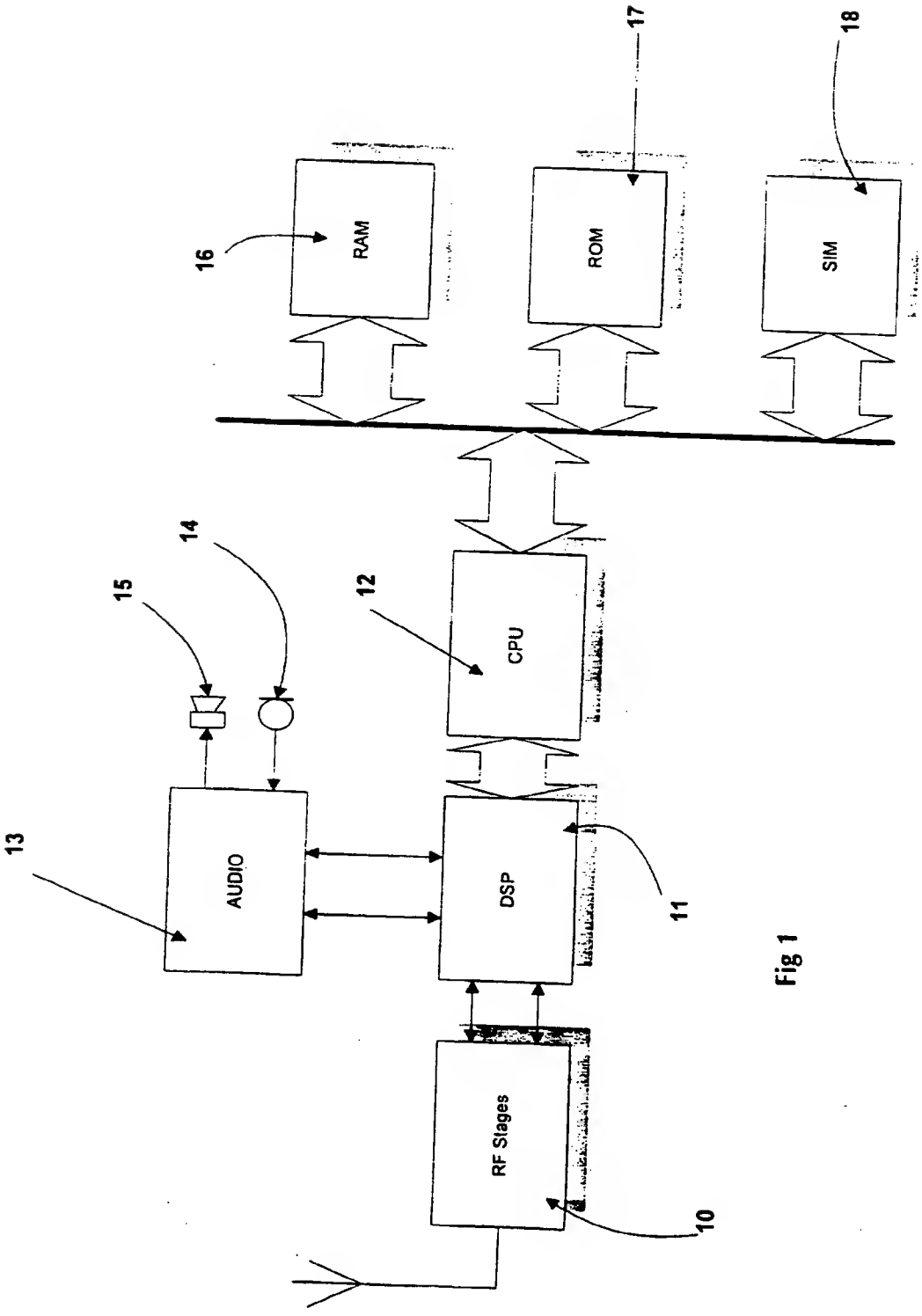

Fig 1

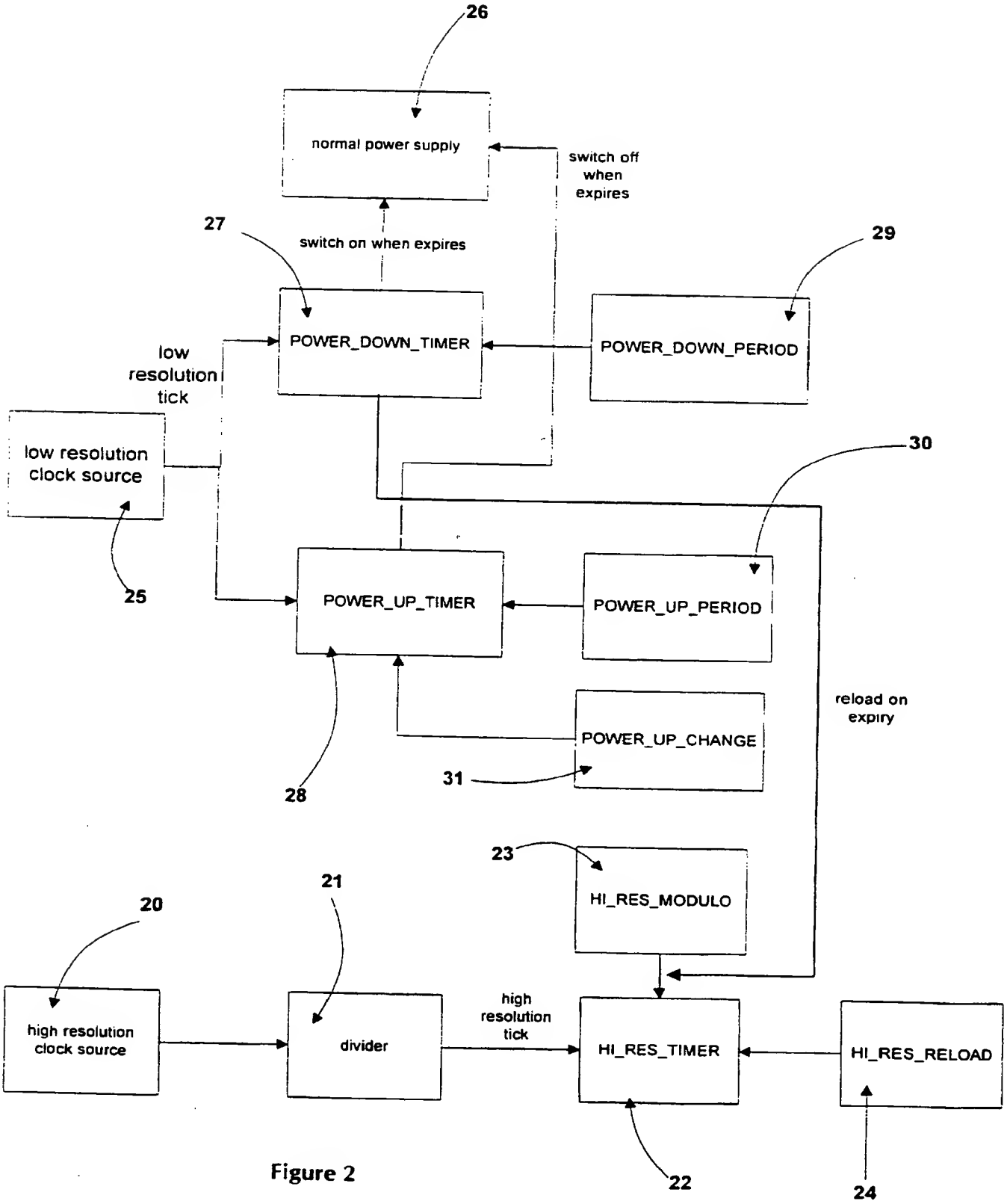
26
normal power supply
switch off when expires
27
switch on when expires
29
POWER_DOWN_TIMER
POWER_DOWN_PERIOD
low resolution tick
low resolution clock source
25
30
POWER_UP_TIMER
POWER_UP_PERIOD
reload on expiry
POWER_UP_CHANGE
28
31
23
HI_RES_MODULO
21
20
high resolution clock source
divider
high resolution tick
HI_RES_TIMER
HI_RES_RELOAD
22
24

Figure 2

High Resolution Clock Reconstruction for Use in a Mobile Telecommunication Device.

This invention relates to the reconstruction of a high resolution clock used in a mobile telecommunication device.

In the GSM or other digital telecommunication system, where time division multiple access (TDMA) is employed to enable a single base station to communicate concurrently with a number of mobile devices, it is very important to ensure that the mobile devices are accurately synchronised with the base station transmissions. To this end, each mobile device includes a stable, accurate, high frequency clock oscillator which is used to measure out time intervals accurately.

The high frequency clock oscillator and the various components used in the high accuracy timing chain are, however, heavy power consumers so that it has become conventional in mobile telecommunication devices to switch off the high frequency clock oscillator and other components of the timing chain periodically to save battery power. It has already been proposed to include in the mobile device a second clock oscillator which runs at a substantially lower frequency and is used in the measurement of the time intervals (hereinafter called "sleep" intervals) during which the high accuracy timing chain is switched off.

In one prior proposal, shortly before a sleep interval commences, the value of a high resolution count is read from a register on an edge of the output of the second oscillator. The high frequency clock oscillator is then switched off for a predetermined number of low frequency clock "ticks" and the device enters a low power or "sleep" mode. At the end

of this interval, the high frequency clock oscillator is started up again. Once the high frequency clock oscillator has switched on and stabilised, the high resolution count register is reloaded with a reconstructed value, which is the value it would have reached had it run continually. This reconstructed value is computed using the formula:

New value = Old value + **TICK_SPEED_RATIO** * **POWER_DOWN_PERIOD**

where

TICK_SPEED_RATIO is the ratio of the frequencies of the two clock oscillators; and

POWER_DOWN_PERIOD is the duration of the sleep interval as measured by the number of ticks of the low frquency clock oscillator.

This solution gives rise to a number of problems. Firstly, the edges of the high frequency clock pulses and the low frequency clock pulses are not synchronous. Moreover, the ratio of the clock frequencies does not have an exact binary representation. Also to be taken into account is jitter on the low frequency clock oscillator edges and variations in the clock speed. Taken together, these factors introduce an error into the reloading of the high resolution count register and these errors are cumulative so that accuracy is lost over an extended period to such an extent that proper operation of the mobile device can no longer be maintained.

It is an object of the present invention to provide a a mobile telecommunications device with a simple arrangement for reconstruction

of the timebase following a sleep interval.

In its broadest aspect, the invention resides a mobile telecommunication device having a high resolution counter which is reloaded at power up following a sleep period with a value derived from a continually running low resolution clock source.

In accordance with the invention there is provided a mobile telecommunication device including a main high frequency, high accuracy clock oscillator, a high resolution counter for counting clock pulses from said main oscillator for controlling the timing of communication operations, a secondary low frequency clock oscillator for timing sleep intervals when said main oscillator is switched off for power conservation purposes, means for cyclically switching the main oscillator on and off periodically for time intervals determined by said secondary clock, and means for loading the high resolution counter with a restart value at the commencement of the on phase each cycle, such restart value being determined in accordance with the restart value in the previous cycle and the total time elapsed (in terms of cycles of the secondary oscillator) since the previous restart.

With this arrangement, cumulative errors in the repeated calculation of the restart value at the commencement of successive cycles do not occur and the high resolution counter can be kept accurately synchronised with signals received from a current base station.

An example of the invention is shown in the accompanying drawings in which:

Figure 1 is a block diagram of a mobile telecommunication device; and

Figure 2 is a block diagram of a high resolution clock reconstruction arrangement in accordance with an example of the present invention.

The device includes RF stages **10**, a digital signal processor (DSP) **11**, and a central processing unit (CPU) **12** . The DSP **11** receives input from the RF stages in the form of analog samples which it processes and stores for use by the CPU **12**. The DSP **11** controls the audio stages **13** of the device and these stages receive microphone **14** input and output audio signals derived from the RF signals received to an ear speaker **15**. The CPU **12** has associated RAM **16** and ROM **17** and there is also a known subscriber identity module **18** which is connected to the CPU.

As shown in Figure 2, the device includes two system clock pulse oscillators. One of these, the main clock pulse oscillator **20** is a high frequency, high accuracy oscillator which operates a frequency of 13MHz. The output of this oscillator is divided down in a divider **21** by a value of 6 to a frequency of 2.1666... MHz which is eight times the bit rate used for the GSM system and is used to clock a high resolution counter **22** the value of the count held in which is referred to hereinafter as **HI_RES_TIMER**. The counter **22** may be a 32-bit counter which operates to count down from a value to which it is reset each time the count has been reduced to zero. This reset value is determined by a value **HI_RES_MODULO** set in a register **23** by the CPU **12**. This value may, for example be eight times the number of bit periods required for a 26-frame GSM multiframe, ie 260000. There is also provision for setting the counter **22** to the value **HI_RES_RELOAD** set in a register **24** by the CPU **12** as will be explained hereinafter.

The system also includes a secondary, lower frequency, low cost oscillator **25** which is used for controlling the duration of sleep periods of the main oscillator and the components associated with it for power saving purposes. When the device is in stand-by mode it needs to receive signals periodically from its currently logged base-station to check for paging signals. These signals occur in precisely defined time slots in the GSM cycle and between these time slots there is no need for the RF stages, the main oscillator, the CPU and other portions of the device to remain active. The function of the secondary oscillator is to provide a means of timing the on and off periods to enable the counter **22** to be loaded with the value it would have held had it not been stopped during the sleep period. Powering down of the main oscillator and the other portions of the device is effected by switching a main power supply unit **26** off.

The oscillator **25** which runs at a frequency of approximately 32KHz drives clocks two counters **27** and **28**. Counter **27** is a power down counter. It is started at a value determined by the value **POWER_DOWN_PERIOD** set in a register **29** at the commencement of a sleep interval and counts down to zero at which time it switches on the power supply **26**. The counter **28** is a power up counter. It is started when the count in the counter **27** reaches zero at a value **POWER_UP_PERIOD** set by the CPU in a register **30**. When the count in counter **28** reaches zero, it switches off the power supply **26** and restarts the counter **27**. The count held in the counter **28** can be changed by the CPU to shorten or lengthen the power up period whilst such period is running. This is done by loading a positive or negative **POWER_UP_CHANGE** value in the register **31**. This value is added to the count of counter **28** on the next occasion it decrements (ie on the

next active edge of the 32KHz clock signal), thus lengthening or shortening the time to expiry whilst maintaining synchronism.

In use, during initialisation of the system a value is read by the CPU from the counter **22** at the appropriate point in the GSM cycle in preparation for a subsequent first sleep period. The secondary clock is also calibrated against the main clock, by counting the number of pulses produced by the divider **21** in a period of 0.5 to 1 second timed by the secondary clock. The value obtained enables the value of a variable **TICK_SPEED_RATIO** to be calculated. This calibration operation is carried out periodically in use to ensure that any frequency drift is allowed for.

In operation the counters **27** and **28** are loaded and clocked alternately by the secondary clock. When a sleep period has expired, the power supply is switched on and the high frequency system is allowed to stabilise by allowing another two or three periods of the secondary clock to elapse, before the **HI_RES_RELOAD** value caculated by the CPU is loaded into the register **24**. The time **ELAPSED**_TIME since the last reload is calculated from the values loaded in the previous cycle into the registers **29** ,**30** allowing for any mid cycle changes made during the power up period and for any additional secondary clock ticks allowed for settling. The value **HI_RES_RELOAD(i)** (ie the value for the ith cycle) is calculated as:

(HI_RES_RELOAD(i-1)+TICK_SPEED_RATIO*POWER_DOWN_PERIOD(i-1))
mod HI_RES_MODULO

The CPU also carries out calculations to maintain a count of the number of multiframes which have elapsed.

It will be noted that none of the calculations carried are dependent on recording a count of the high resolution clock pulses during operation, except for the purposes of obtaining one initial value of **HI_RES_RELOAD(0)** during initialisation and for periodic calibration of the secondary clock. Calibration is carried out over a sufficiently long interval to obtain the ratio to the necessary level of precision. Whilst there will be a small error in the reload value on each reload these errors are random and will not be cumulative.

CLAIMS

1. A mobile telecommunication device having a high resolution counter which is reloaded at power up following a sleep period with a value derived from a continually running low resolution clock source.

2. A mobile telecommunication device including a main high frequency, high accuracy clock oscillator, a high resolution counter for counting clock pulses from said main oscillator for controlling the timing of communication operations, a secondary low frequency clock oscillator for timing sleep intervals when said main oscillator is switched off for power conservation purposes, means for cyclically switching the main oscillator on and off periodically for time intervals determined by said secondary clock, and means for loading the high resolution counter with a restart value at the commencement of the on phase of each cycle, such restart value being determined in accordance with the restart value in the previous cycle and the total time elapsed (in terms of cycles of the secondary oscillator) since the previous restart.

3. A mobile telecommunication device as claimed in claim 2 in which said high resolution counter is cyclically reset to a modulo value which is also taken into account in the calculation of the restart value.

4. A mobile telecommunication device as claimed in claim 2 or claim 3 in which said means for cyclically switching the main oscillator on and off, comprises first and second counters periodically loaded respectively with count values representing the required durations of the on and off periods, the first counter acting on expiry to switch the main oscillator off and start the second counter and the second counter acting

on expiry to switch the main oscillator on and start the first counter.

5. A mobile telecommunication device as claimed in claim 4 in which there are provided first and second registers which are loaded with on and off duration values by a central processor unit and from which the first and second counters are loaded respectively.

6. A mobile telecommunication device as claimed in claim 5 in which there is provided a further register which is loaded with a change value by the CPU when it is required to change the on duration during the on phase, the change value being added to the current count ohaving a high resolution counter which is reloaded at power up following a sleep period with a value derived from a continually running low resolution clock source.

The Patent Office

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Claims searched:	All	**Date of search:**	21 January 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G4H (HRCA, HRCZ, HRZ), H4L (LECTP)

Int Cl (Ed.6): H04M 1/72, H04Q 7/18, 7/32

Other: Online Database: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB2297884 A	(NOKIA) p.10 line 3 - p.12 line 2	1 at least
X	GB2297854 A	(NOKIA) p.9 line 6 - p.11 line 7	1 at least
X	EP0758768 A2	(ROCKWELL) col.5 line 7 - col.6 line 58	1 at least
X	EP0586256 A2	(NOKIA) whole document	1 at least
X	WO95/10141 A1	(MOTOROLA) p.5 line 25 - p.11 line 22	1 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.